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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,407	02/04/2004	Anthony J. Magrath	M0025.0302/P302	2733

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DICKSTEIN SHAPIRO LLP  
1825 EYE STREET NW  
Washington, DC 20006-5403

EXAMINER
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BOCURE, TESFALDET

ART UNIT	PAPER NUMBER
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2611

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/05/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

10/770,407

Applicant(s)

MAGRATH, ANTHONY J.

Examiner

Tesfaldet Bocure

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,5,7 and 21 is/are rejected.
- 7) ☐ Claim(s) 2-4,6 and 8-20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 2/04/04 & 3/23/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The Information Disclosure Statements (IDSs) received on 2/04/04 and 3/23/2004 have been received and the initialed copies (two pages) of the IDSs are attached with this correspondence.

### ***Drawings***

3. Figures 1-4 have been disclosed in the "background of the invention" as conceptual figures, which are not sure whether they are prior art or not—clarification required.

### ***Specification***

4. The incorporation of essential material in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing

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the applicant, stating that the material being inserted is the material previously incorporated by reference and that the amendment contains no new matter. 37 CFR 1.57(f).

5. The attempt to incorporate subject matter into this application by reference to "Delta sigma Data Converters, theory, Design and Simulation" by Steven et al. disclosed in page 18 with respect to fig. 7 is ineffective because the subject matter shown in figure 7 is critical to the claimed subject matter in claims 1-19.

6. The disclosure is objected to because of the following informalities: It is confusing that application discloses in page 18, second paragraph to the subject matter in shown in fig. 7 and in the third paragraph without referring back to figure 6 the subject matter shown in fig. 6. Examiner is kindly requesting applicant to make reference to fig. 6 to the disclosed subject matter in the third paragraph (paragraph starting ---In the case where bit flipping-- in page 18.

Appropriate correction is required.

### ***Claim Objections***

Claims 5 and 7 are objected to because of the following informalities: Claim 5: It is not understood from the claim what is meant by "to remove double said feedback portion."

Claim 7: The claimed "provides the or" in line 7 need to be revised.

Appropriate correction is required.

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7. Claims 16 and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16: "Said differences" in lines 4-5 lack clear antecedent basis.

Claims 18-20 are inherently rejected as being dependent on the rejected base claim.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Magrath et al., Magrath hereinafter (Design and Implementation of a FPGA Sigma-Delta Power DAC).

Magrath hereinafter teaches a delta sigma modulator with bit flipping (figs 2 and 4) and look-ahead block (fig.4) comprising: A bit-flipping sigma-delta modulator for a class D amplifier and comprising:

a quantiser (Q) coupled to a bit-flipping means (BF); one or more look-ahead quantisers (PRF); and a controller (Controller) having inputs from the quantiser and the look-ahead quantizer and arranged to enable the bit-flipping means (see output from the Look Ahead to PRF) to provide a different output from that of the quantiser in

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order to reduce the quantized output transition rate of the modulator (see also page 513);

a feedback circuit arranged to add a portion of the quantiser output to the input signal path Of the modulator (see feedback output from the control unit to summer and filter), and further comprising an integrator circuit (see integrator with mux in fig. 4) in the input signal path between the input and the quantiser, the integrator circuit having a compensation circuit for adjusting the input to the quantiser when said previous modulator output has been changed by the bit flipping means from said previous.

Further to claim 7, the modulators shown in figures 2 and 4 are bi-level modulator receiving and processing two level signals (-1 and 1 shown in fig.3) and bit flipping block (BF) block provides a different output by flipping output bit-sequences from the quantizer (Q) as shown in fig. 3.

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Magrath et al., Magrath hereinafter (Design and Implementation of a FPGA Sigma-Delta Power DAC).

Magrath teaches the claimed subject matter claimed in claim 1 as indicated above.

What Magrath fails to teach is that the delta-sigma modulator shown in figs 2 and 4 as being class D- amplifier as in claim 1. Such a class D-amplifiers for implementing a Delta-Sigma Modulation is widely and notoriously known<sup>1</sup> for converting the received high bit rates bits to high frequency low bit rate and Examiner is taken an official notice.

Therefore, it would have been obvious to one of an ordinary skill in the art to use a class D-amplifier for use in a delta sigma modulation technique to convert high bit rate received pulses into low bit rate pulse at the time the invention was made.

#### ***Allowable Subject Matter***

12. Claims 2-4,6 and 8-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Publications: "Resolution Enhancement and Dither of Sigma-

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Delta Modulator Digital-to-analogue Converters” and “Non-Linear Deterministic Dithering of Sigma-Delta Modulators” by Magrath et al. disclose a delta-sigma-modulator having bit-flipping block. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tesfaldet Bocure whose telephone number is (571) 272-3015. The examiner can normally be reached on Mon-Thur (7:30a-5:00p) & Mon.-Fri (7:30a-5:00p).

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti (Jay) Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

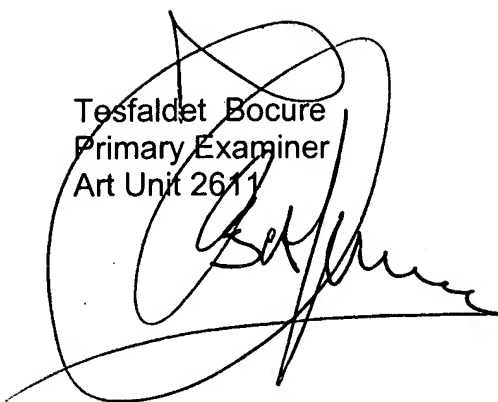
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<sup>1</sup> To mention few, see for example US patent publication numbers 2004/0207465 and 2004/0066228



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Tesfaldet Bocure  
Primary Examiner  
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A large, stylized handwritten signature in black ink, overlapping the printed name and title of the examiner.

T.Bocure

16.